Basic Hardware Interfacing

Purpose:
To become acquainted with external hardware interfacing techniques.

Drive LEDs on external prototype board. Receive signal input (push button switch) from prototype circuit board.

Points to Consider:
1) PIC development board is a 3.3V system. A lot of common logic circuitry, TTL, runs from 5V system. Electric motors can run up to +/-24V system or more. How to translate signals from one system to another?
2) Even PIC development board digital I/O pins can drive/pull 20mA, in lab environment we prefer to buffer, so provide additional protection.

Procedure:

1) Use portA to provide 1 digital out signal and 1 digital in signal
2) PortA is multiplexed with the JTAG function and RA4, RA5, RA0, RA1 are available on that connector.
3) The output signal will go off board to a solderless prototype board, through an optical isolator and than a 7405 TTL open collector driver to drive an LED.
4) The input signal will come off prototype board to Dev. Board from optical isolator from pushbutton switch.
5) The software will sense when the push button switch is pressed and than blink the leds in the following order: external PortA, LED3, LED2, LED1 on PIC32 starter kit.
6) Be sure you learn and understand how to use the optical isolators. We will use them many, many, many more times in the future.
7) Check off your project by demo-ing its function to TA.

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Single-Channel: 6N138, 6N139
Dual-Channel: HCPL2730, HCPL2731
Low Input Current High Gain Split Darlington Optocouplers

Features
- Low current - 0.5mA
- Superior CTR-2000%
- Superior CMR-10kV/μs
- CTR guaranteed 0–70°C
- U.L. recognized (File # E90700)
- VDE recognized (File # 120915) Ordering option V, e.g., 6N138V
- Dual Channel – HCPL2730, HCPL2731

Applications
- Digital logic ground isolation
- Telephone ring detector
- EIA-RS-232C line receiver
- High common mode noise line receiver
- uP bus isolation
- Current loop receiver

Description
The 6N138/9 and HCPL2730/HCPL2731 optocouplers consist of an AlGaAs LED optically coupled to a high gain split darlington photodetector. The split darlington configuration separating the input photodiode and the first stage gain from the output transistor permits lower output saturation voltage and higher speed operation than possible with conventional darlington phototransistor optocoupler. In the dual channel devices, HCPL2730/HCPL2731, an integrated emitter-base resistor provides superior stability over temperature. The combination of a very low input current of 0.5mA and a high current transfer ratio of 2000% makes this family particularly useful for input interface to MOS, CMOS, LSTTL and EIA RS232C, while output compatibility is ensured to CMOS as well as high fan-out TTL requirements. An internal noise shield provides exceptional common mode rejection of 10 kV/μs.

Schematic

Package Outlines
DM74LS05
Hex Inverters with Open-Collector Outputs

General Description
This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations
\[
R_{\text{MAX}} = \frac{V_{\text{CC}} \text{ (Min)} - V_{\text{OH}}}{N_1 \text{ (IOH)} + N_2 \text{ (IOL)}}
\]
\[
R_{\text{MIN}} = \frac{V_{\text{CC}} \text{ (Max)} - V_{\text{OL}}}{I_{\text{OL}} - N_3 \text{ (IL)}}
\]

Where:
- \( N_1 \) (IOH) = total maximum output high current for all outputs tied to pull-up resistor
- \( N_2 \) (IOL) = total maximum input high current for all inputs tied to pull-up resistor
- \( N_3 \) (IL) = total maximum input low current for all inputs tied to pull-up resistor

Ordering Code:

<table>
<thead>
<tr>
<th>Order Number</th>
<th>Package Number</th>
<th>Package Description</th>
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</thead>
<tbody>
<tr>
<td>DM74LS05M</td>
<td>M14A</td>
<td>14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow</td>
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<tr>
<td>DM74LS05SJ</td>
<td>M14D</td>
<td>14-Lead Small Outline Package (SOJ), EIAJ TYPE II, 5.3mm Wide</td>
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<tr>
<td>DM74LS05N</td>
<td>N14A</td>
<td>14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-061, 0.300 Wide</td>
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</tbody>
</table>

Function Table

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
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</thead>
<tbody>
<tr>
<td>( A )</td>
<td>( \bar{A} )</td>
</tr>
<tr>
<td>( L )</td>
<td>( H )</td>
</tr>
<tr>
<td>( H )</td>
<td>( L )</td>
</tr>
</tbody>
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H = HIGH Logic Level
L = LOW Logic Level