Practice 1: The Basic Op-Amp Amplifier

[Prolog] We will look at using the op-amp to design a basic amplifier. Op-amp can be used to design amplifiers, comparators, or “hybrid” circuits. The ideal basic op-amp amplifier circuit analysis assumes the following:

1. \( I_{(+)} = I_{(-)} = 0 \), i.e. none of the 2 input terminals draws current. This actually coincides with the ideal op-amp property.

2. \( V_{(+)} = V_{(-)} \), i.e. input voltages are the same for both terminals. This is true only when we are looking at using op-amp to design an amplifier.

As you can see, (1) and (2) rely a lot on the “idealness” of the design as well. In reality, we should not assume the op-amp to be ideal when:

a. The required gain is too large (e.g. > 1000)
b. Input voltages are too small (< 100 mV)
c. Operating frequency is too high (> 100 KHz)
d. Wave form “climbs” or “drops” too fast
e. Large voltage or large current outputs
f. DC level measurement is considered (DC non-idealness)

Now let’s look at some basic amplifier circuits.

1. Inverting Amplifier

(1) Construction

\[
V_o = -(R_2/R_1)V_s
\]
\[
A_{vo} = V_o / V_s = -(R_2/R_1)
\]

The – sign indicates that this is an inverting amplifier, i.e. the gain is negative. Also:

\( R_{in} \), the input impedance, = \( V_s / I_1 = R_1 \), where \( I_1 \) is the current through \( R_1 \).

\( R_{iA} \equiv R_1 \)
\( R_{iB} \equiv 0 \)
\( R_{iC} \equiv \) several \( M\Omega \)
(2) Determining \( R_1 \) and \( R_2 \) values

Since we need to “pass on” the input voltage when amplifying, \( R_1 \) cannot be too small. \( R_1 \) and \( R_2 \) cannot be too large either. See the figure below when using the amplifier at high frequency. At high frequencies, there exists parasitic capacitance at input \( (C_i) \) and also within the feedback loop \( (C_f) \). These capacitances degrade the response of the amplifier. There are other less major reasons as well.

2. Non-inverting Amplifier

(1) Construction:

This circuit will raise the input impedance to \( \gg M\Omega \) and lower the output impedance to \( \approx 0\Omega \), i.e. it is a good design!

\[
V_o = (1 + R_2/R_1) \cdot V_s
\]

\( \Leftarrow \) Can you see why?

\[
A_{vo} = V_o / V_s = (1 + R_2/R_1)
\]

3. Voltage Follower

(1) Construction
If you examine this circuit, you will see that this circuit is equivalent to a non-inverting amplifier with \( R_1 = \infty \) and \( R_2 = 0 \). Thus, using the non-inverting amplifier’s equations, we obtain that \( V_o = (1 + 0) V_s = V_s \) and \( A_{vo} = 1 \).

(2) Reducing the loading effect

We use the voltage follower as “buffers” between the input signal and the load to reduce the loading effect. Below is a figure showing how this works.

On the left, voltage division using the two resistors gives us 5V. In the middle, directly adding the load \( R_L \) gives us 2.14V using voltage division as well. But what we need is to hold the 5 V and not let it drop to 2.14V. On the right, by first adding the buffer then adding the load \( R_L \) we get the 5V as desired.

(3) Other Practical Use Concerns

There are some practical concerns in the realistic use of the voltage follower. First, it’s safety. Because there is time delay between the op-amp’s input and output, when using V.F. to process fast increasing or fast decreasing input signals, the op-amp’s 2 input terminals will show a large voltage difference. This can damage the op-amp’s input transistor’s base-emitter construction. To address, we use diodes to limit the input difference, as seen below on the left side:

The second problem is the non-ideal DC characteristics of the op-amp (a whole subject all by itself!) Typically we add a resistance \( R_F \) in series, and a capacitance \( C_F \) in parallel within the feedback loop to cope with this, as shown on the right side above.