EE 4429 – Advanced Electronics

Midterm Exam

October 28, 2014 (3:00 – 5:00 p.m.)

Your Name: ____________________                     Total Points: _________

Last 5 of Bengal ID: _________________

There are 4 groups of questions. Full score is 100 points. For maximum credit, show and organize all your work neatly.

Topics covered in this Midterm Exam include:

A. Diode detector circuit and applications (25 points)
B. DC biasing of multistage BJT circuits (35 points)
C. BJT amplifier design and analysis (25 points)
D. CMOS logic function implementation (15 points)
Q1. Given the input signal and the diode circuit below:

![Image of diode circuit](image)

a. (15 points) Assuming that the RC time constant of this circuit is approximately equal to the period of the input signal $v_{in}$, plot the output signal $v_{OUT}$ and justify your answer in details.

If RC time constant is approximately the period of $v_{in}$, $v_{OUT}$ will be able to catch the peak values of $v_{in}$. But $v_{OUT}$ will not follow $v_{in}$, because it will “drop” before each peak of $v_{in}$.

![Image of output signal](image)

b. (10 points) What will happen if the RC time constant is too large, i.e. much larger than the period of the input signal $v_{in}$?

For this application, the RC time constant should be approximately equal to the period of the carrier signal, so that the output voltage can follow each peak value of the carrier signal. If the time constant is too large, the output will not be able to change fast enough and the output will not represent the audio output. Only few peaks of $v_{in}$ will be represented in $v_{OUT}$.
Q2. Consider the following multistage circuit. Assume that for the transistors Q₁ and Q₂, β = 100 and $V_{BE(ON)} = 0.7$ V.

![Circuit Diagram]

a. (25 points) Calculate, by hand, the DC voltages at each node, and the DC currents through all the circuit elements.

Considering the circuit below, the Thevenin resistance and voltage are:

$$R_{TH} = R_1 || R_2 = 100 || 50 = 33.3 \text{ kΩ}$$

and

$$V_{TH} = \left( \frac{R_2}{R_1 + R_2} \right)(10) - 5 = \left( \frac{50}{150} \right)(10) - 5 = -1.67 \text{ V}$$

Kirchhoff’s voltage law equation around the B–E loop of Q₁ is

$$V_{TH} = I_{B1} R_{TH} + V_{BE \text{ (on)}} + I_{E1} R_{E1} - 5$$
Noting that \( I_{E1} = (1 + \beta)I_{B1} \), we have

\[
I_{B1} = \frac{-1.67 + 5 - 0.7}{33.3 + (101)(2)} \Rightarrow 11.2 \, \mu \text{A}
\]

Therefore,

\[
I_{C1} = 1.12 \, \text{mA}
\]

and

\[
I_{E1} = 1.13 \, \text{mA}
\]

Summing the currents at the collector of \( Q_1 \), we obtain

\[
I_{R1} + I_{B2} = I_{C1}
\]

which can be written as

\[
\frac{5 - V_{C1}}{R_{C1}} + I_{B2} = I_{C1}
\]

\[
I_{B2} = \frac{I_{E2}}{1 + \beta} = \frac{5 - V_{E2}}{(1 + \beta)R_{E2}} = \frac{5 - (V_{C1} + 0.7)}{(1 + \beta)R_{E2}}
\]

Note also that \( I_{C1} = \beta I_{B1} \) and \( I_{E1} = I_{C1} + I_{B1} \).
\[
\frac{5 - V_{C1}}{R_{C1}} + \frac{5 - (V_{C1} + 0.7)}{(1 + \beta)R_{E2}} = I_{C1} = 1.12 \text{ mA}
\]

which can be solved for \( V_{C1} \) to yield

\[ V_{C1} = -0.482 \text{ V} \]

Then,

\[ I_{R1} = \frac{5 - (-0.482)}{5} = 1.10 \text{ mA} \]

To find \( V_{E2} \), we have

\[ V_{E2} = V_{C1} + V_{EB\text{(on)}} = -0.482 + 0.7 = 0.218 \text{ V} \]

The emitter current \( I_{E2} \) is

\[ I_{E2} = \frac{5 - 0.218}{2} = 2.39 \text{ mA} \]

Then,

\[ I_{C2} = \left( \frac{\beta}{1 + \beta} \right) I_{E2} = \left( \frac{100}{101} \right) (2.39) = 2.37 \text{ mA} \]

and

\[ I_{B2} = \frac{I_{E2}}{1 + \beta} = \frac{2.39}{101} \Rightarrow 23.7 \text{ \( \mu \)A} \]

The remaining nodal voltages are

\[ V_{E1} = I_{E1} R_{E1} - 5 = (1.13)(2) - 5 \Rightarrow V_{E1} = -2.74 \text{ V} \]

and

\[ V_{C2} = I_{C2} R_{C2} - 5 = (2.37)(1.5) - 5 = -1.45 \text{ V} \]

We then find that

\[ V_{CE1} = V_{C1} - V_{E1} = -0.482 - (-2.74) = 2.26 \text{ V} \]

and that

\[ V_{EC2} = V_{E2} - V_{C2} = 0.218 - (-1.45) = 1.67 \text{ V} \]
Q3. (25 points) Consider the following amplifier circuit. Assume that for the transistor, $\beta = 100$ and $V_{BE(ON)} = 0.7$ V. Find the values of $R_C$, $R_{E1}$ and $R_{E2}$ such that an input sinusoid of 12 mV is amplified to a 0.4 V sinusoidal output.

*You may choose any logical Q-point $I_C$ and $V_{CE}$.*

**Solution (Initial Design Approach):** The magnitude of the voltage gain of the amplifier needs to be

$$|A_v| = \frac{0.4\text{ V}}{12\text{ mV}} = 33.3$$

From Equation (6.59), the approximate voltage gain of the amplifier is

$$|A_v| \approx \frac{R_C}{R_{E1}}$$

Noting from the last example that this value of gain produces an optimistically high value, we can set $R_C/R_{E1} = 40$ or $R_C = 40 R_{E1}$.

The dc base-emitter loop equation is

$$5 = I_B R_B + V_{BE(on)} + I_E(R_{E1} + R_{E2})$$

Assuming $\beta = 100$ and $V_{BE(on)} = 0.7$ V, we can design the circuit to produce a quiescent emitter current of, for example, 0.20 mA. We then have

$$5 = \left(\frac{0.20}{100}\right) + 0.70 + \left(\frac{0.20}{R_{E1} + R_{E2}}\right)$$

which yields

$$R_{E1} + R_{E2} = 20.5\text{ k}\Omega$$

Assuming $I_E \approx I_C$ and designing the circuit such that $V_{CEQ} = 4$ V, the collector–emitter loop equation produces

$$5 + 5 = I_C R_C + V_{CEQ} + I_E(R_{E1} + R_{E2}) = (0.2)R_C + 4 + (0.2)(20.5)$$

or

$$R_C = 9.5\text{ k}\Omega$$

Then

$$R_{E1} = \frac{R_C}{40} = \frac{9.5}{40} = 0.238\text{ k}\Omega$$

and $R_{E2} = 20.3\text{ k}\Omega$. 
Q4. (15 points) Using CMOS, implement a logic function \( Y = AB + C(D+E) \). Assume that A, B, C, D and E are available as input signals. Start with the following diagram, in which the input signals are applied to both the PMOS and NMOS networks.

Fully specify, using appropriate transistors, what should be in the PMOS and NMOS networks. (Hint: The input signals are to be applied to the gates of the CMOS transistors.)

This CMOS circuit implements \( V_O = Y' \).