MOSIS

- A low-cost prototyping service
- Collects designs from academic, commercial, and government customers
- Aggregates the designs onto 1 mask set
- Shares overhead costs
- Generates production volumes to interest foundries
- Specifies a set of scalable $\lambda$-based DR's covering a wide range of processes
- These DR's describe:
  - Minimum width to avoid breaks in a line
  - Minimum spacing to avoid shorts between lines
  - Minimum overlap to ensure that 2 layers overlap completely

Some of these major DR's for 2 metal layers in an n-well process are:

- Metals (blue stripes) and diffusion (in gray) use $4\lambda$ as width and spacing
- Contacts (black) are $2\lambda$ by $2\lambda$, and must be surrounded by $1\lambda$ for layers
- Polysilicon (black stripes) width is $2\lambda$ and spacing is $3\lambda$ ($1\lambda$ w/o transistor)
- Polysilicon and contacts use $3\lambda$ spacing
- N-well surrounds pMOS transistors by $6\lambda$, and avoids nMOS by $6\lambda$ also
- Recall that $\lambda = \frac{1}{2}$ feature size (distance between Drain and Source)

The following diagram was from our previous Lect0-#40, showing these DR's:
If you have 3 metal layers, then the width of the 3rd layer is typically $6\lambda$, and the spacing will be $4\lambda$. The more layers you have, the thicker and wider the top-level metal will be (to provide lower resistance).

**W/L ratio**

- In the above diagram, where polysilicon crosses n-diffusion, $W/L = 4\lambda/2\lambda$.
- This means, for a 0.6-μm process, $W = 1.2\mu m$ and $L = 0.6\mu m$.
- This minimum-width transistor is also called a *unit transistor*.
- pMOS transistors tend to double the size of nMOS transistors, $W/L = 8\lambda/2\lambda$.
- In digital systems, we often minimize $L$ for better speed, area, and power.

**Gate layout**

- No quick and dirty ways for best designs.
- Simple “line of diffusion” rule most common for automated layout design.
- 4 horizontal strips in a cell:
  - Metal ground at the bottom (a supply rail)
  - N-diffusion
  - P-diffusion
  - Metal power at the top (another supply rail)
  - Polysilicon lines run vertically to form transistor gates
  - Metal wires connect the transistors as designed
- P-substrate is tied to ground (substrate tap).
- N-well is tied to power (well tap).

**Stick diagrams**

- Free the designers from having to worry about scale.
- Great for using markers, crayons, or colored pencils.
- Still easy to estimate area (e.g. $32\lambda$ by $40\lambda$).
- Layout area is mainly determined by the metal wires.
- **Routing Track**: space for placing a wire.
- Pitch: wire width + spacing to the next wire.
- Minimum pitch is typically $8\lambda$. (4λ. width + 4λ. spacing).
- Estimate cell width/height as $8\lambda\ast$(# of metal tracks).
- **Well Spacing**: 12λ. between nMOS and pMOS (8λ + 4λ).
- Essentially, count the number of wire tracks.